DRAWINGS MANUAL

ADAM
ADVANCED DIGITAL AUDIO MATRIX

AUDIO I/O CARD

RTS™

9300-7510-500 REV C

08/2003

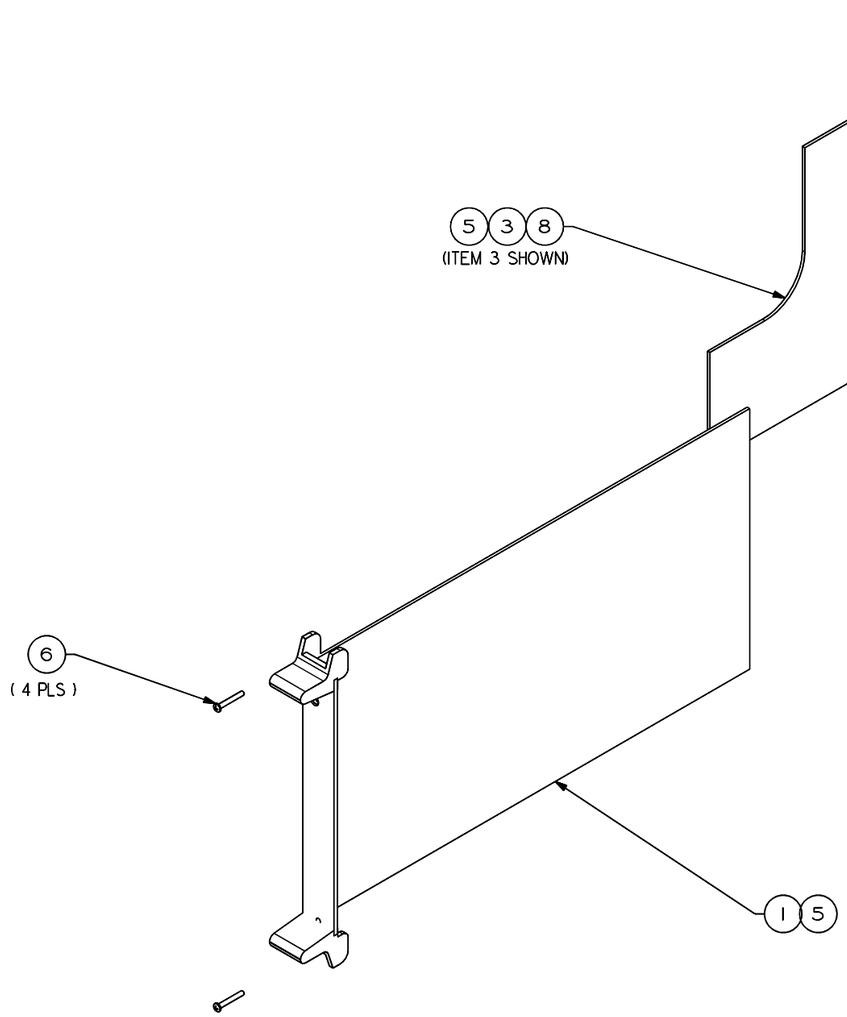
NOTES:

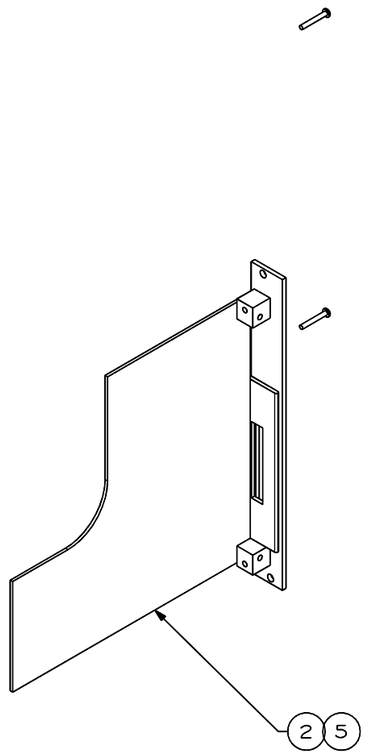
2	SHEET
	REV.

SHEET REVISION STATUS

REVISIONS

LOC.	REV.	DESCRIPTION	ECO. NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	61487	dk	--	TAY	2-8-96
	B	ADD ITEMS 6 & 7	61906	dk	--	--	6-7-96
	C	ADD -002. ITEM 8	73077	KS	KS	--	4-25-00





-004 QTY.	-003 QTY.	-002 QTY.	-001 QTY.	-000 QTY.	ITEM NO.	REF. DESIG.	PART NUMBER	DESCRIPTION
		1			8		90207688-000	ANALOG I/O BACKCARD ASSY. RJI2
		1	1	1	7		00658-000	BAG. PLASTIC
		4	4	4	6		59000-240	SCREW. PANHEAD. M2.5 X 10.0
		AR	AR	AR	5		56406-001	ANTI-STATIC BAG TUBING
		1	1	1	4		93106910-000	CARTON
			1		3		90207512-000	ANALOG I/O BACKCARD ASSY. RJ45
				1	2		90207511-000	ANALOG I/O BACKCARD ASSY. SCSI
		1	1	1	1		90207510-000	ANALOG I/O FRONT CARD ASSY

LIST OF MATERIALS

CAD GENERATED DRAWING
PROJECT: ADAM
SUBPROJECT: MAINFRAME
OBJECT: KT_AIO

MODEL	NEXT ASS'Y
ADAM	90007500

UNSPECIFIED LIMITS OF TOLERANCE
STRAIGHTNESS AND/OR FLATNESS .005 IN./1 IN.
CONCENTRICITY .010 TIR
ANGLES ±1/2° BENDS ±2°
UNMARKED ANGLES, BENDS AND INTERSECTIONS 90°
THREADS- EXT. CLASS 2A INT. CLASS 2B
MOLD FINISH: SPI-SPE NO 3
DRAFT: 2°
DECIMAL
.X ±.050 IN.
.XX ±.030 IN.
.XXX ±.010 IN.
MACHINED FINISH: 64

DR	dk	CK		APP	
DATE	2-6-96	SCALE	NONE		

DO NOT SCALE DRAWING

TELEX.
MINNEAPOLIS, MINNESOTA

TITLE: AIO-ADAM-KIT

SIZE	DWG. NO.
D	90027510
	SHT 1 OF 1

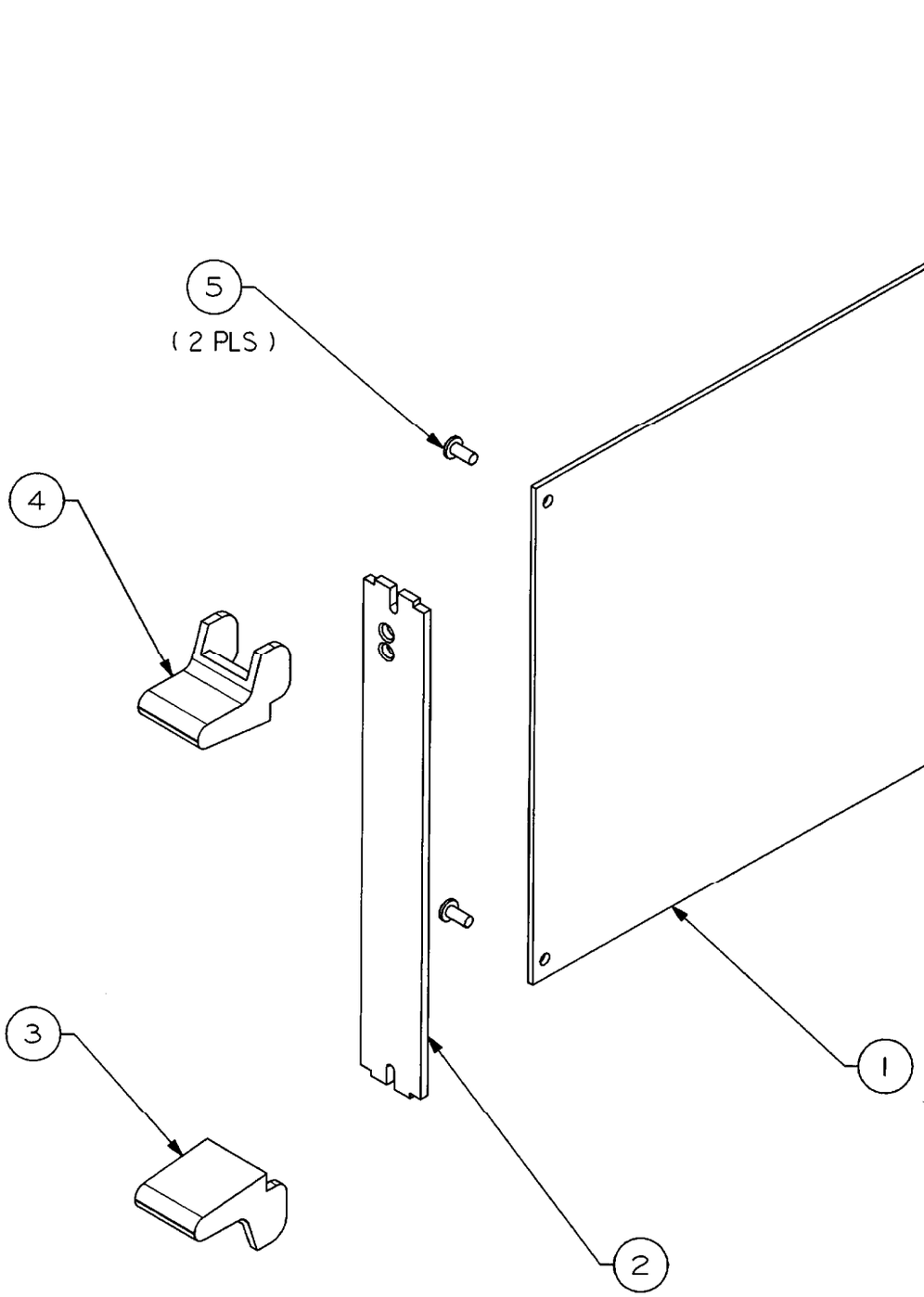
PLANT DIST. LN

NOTES:

2	SHEET
	REV.

SHEET REVISION STATUS

REVISIONS							
LOC.	REV.	DESCRIPTION	ECO. NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	61487	dk		CWT	2-8-96
	B	CHNG P/N ITEM 5 WAS 51845-038	62388	dk	--	--	10-18-96
	C	ADD ITEM 6	63468	JC	JC	--	5-1-98



-004 QTY.	-003 QTY.	-002 QTY.	-001 QTY.	-000 QTY.	ITEM NO.	REF. DESIG.	PART NUMBER	DESCRIPTION
				AR	6		879039	BE BOXING ASSEMBLY
				2	5		59000-230	SCREW. METRIC
				1	4		59019I-000	EXTRACTER
				1	3		59019I-001	EXTRACTER
				1	2		91107467-001	CARD PLATE. FRONT
				1	1		90307510-000	ADAM ANALOG I/O PC BOARD ASSY

LIST OF MATERIALS

CAD GENERATED DRAWING
PROJECT: ADAM
SUBPROJECT: MAINFRAME
OBJECT: AIO_8_FC

ADAM	90027510
MODEL	NEXT ASS'Y

UNSPECIFIED LIMITS OF TOLERANCE
STRAIGHTNESS AND/OR FLATNESS .005 IN./1 IN.
CONCENTRICITY .010 TIR
ANGLES ±1/2° BENDS ±2°
UNMARKED ANGLES, BENDS AND INTERSECTIONS 90°
THREADS- EXT. CLASS 2A INT. CLASS 2B
DECIMAL .X ±.050 IN. .XX ±.030 IN. .XXX ±.010 IN.
MACHINED FINISH: 64
MOLD FINISH: SPI-SPE NO 3
DRAFT: 2°

DR dk | CK | APP
DATE 12-23-96 | SCALE 1 : 1
DO NOT SCALE DRAWING

TITLE AIO-8-FC

TELEX®
MINNEAPOLIS, MINNESOTA

SIZE C | DWG. NO. 90207510 | SHT 1 OF 1

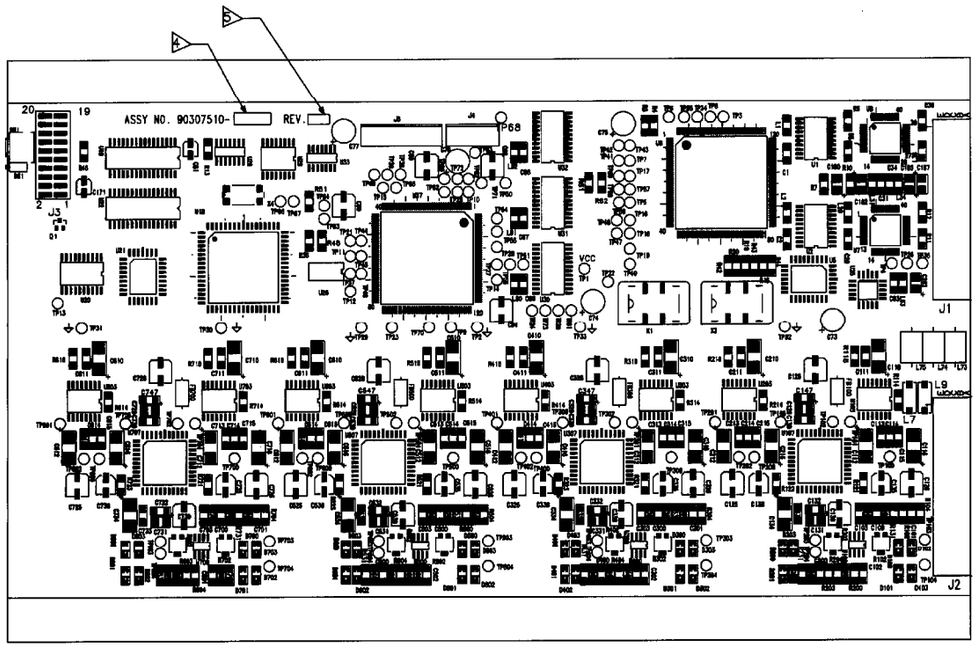
PLANT DIST. LN. BE

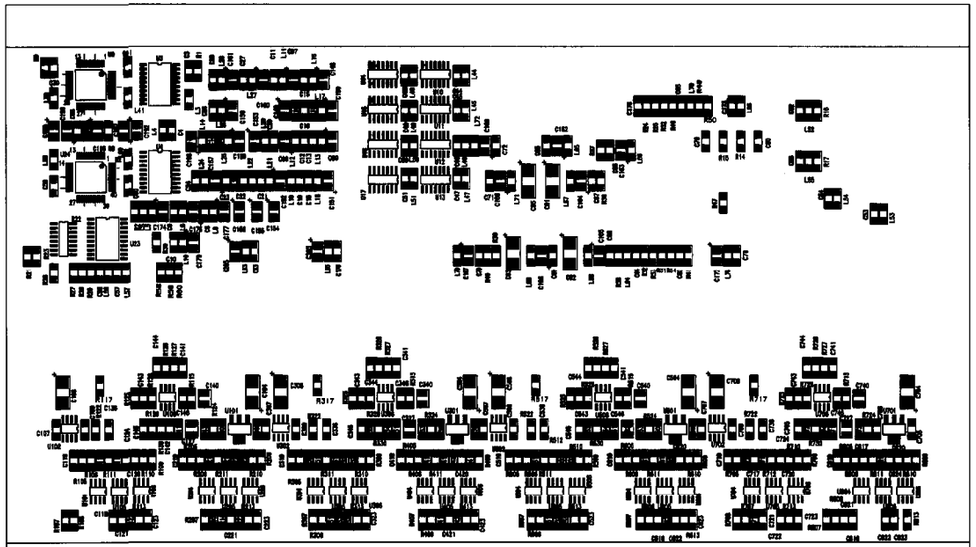
					SHEET	SHEET REVISION STATUS
					REV.	

REVISIONS

LOC.	REV.	DESCRIPTION	ECO. NO.	DRFT	CHKR	APP	DATE
	E	REVISED AND REDRAWN	63487	CBH			6/12/98
	F	CHANGED NOTES 2 &3.	63641	CBH			2/4/99
	G	CHANGED NOTE 3.	63653	CBH			3/10/99

NOTES:
1. MANUFACTURING TO STAMP REV ON BOARD THAT APPEARS ON DRAWING
2. REFERANCE SCHEMATIC DRAWING 90277510-000 REV F
3. PARTS LIST FILED SEPARATLY 90307510-000 REV G
   90307510-500 REV G
4. WRITE ASSEMBLY VERSION BUILT TO WHERE SHOWN.
5. WRITE ASSEMBLY REV BUILT TO WHERE SHOWN.





-004 QTY.	-003 QTY.	-002 QTY.	-001 QTY.	-000 QTY.	ITEM NO.	REF DESIG.	PART NUMBER	DESCRIPTION
					REV	LIST OF MATERIALS		

UNSPECIFIED LIMITS OF TOLERANCE
STRAIGHTNESS AND/OR FLATNESS .003 IN/1 IN.
CONCENTRICITY .010 TIR
ANGLES P1/2D BENDS P2D
UNMARKED ANGLES, BENDS AND INTERSECTIONS 90D
THREADS- EXT. CLASS 2A INT. CLASS 2B
MOLD FINISH: SPI-SPE NO. 3
DRAFT 2D

DECIMAL
.X P.050 IN.
.XX P.030 IN
.XXX P.010 IN.

MACHINED FINISH: 64

DR CBH
DATE
SCALE 1:1
DO NOT SCALE DRAWING

TELEX.
MINNEAPOLIS, MINNESOTA

TITLE
ADAM ANALOG I/O CARD
ASSEMBLY DRAWING

P/N
SIZE D
DWG. NO. 90307510
SHT. 1 OF 1
PLANT DIST. B.E.

CAD GENERATED DRAWING
FILE NAME:\IC_GROUP\BOARDS\7510\REVF\7510F.PCB

MODEL	NEXT ASS'Y

NOTES:

1. ALL RESISTORS TO BE OHMS, 1/8W, 5%, UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS TO BE UF UNLESS OTHERWISE SPECIFIED.
3. LAST REF DES USED: C824,D803,DS1,J5,L85,Q1,RP14,SW2,TP804,U805,X4
4. NOT STUFFED FOR ADAM CS (-500)
5. NOT STUFFED FOR ADAM (000)

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	SHEET
C	D	D	D	D	D	D	D	D	D	D	D	D	D	C	C	C	D	D	REV.

SHEET REVISION STATUS

REVISIONS							
LOC	REV	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE WAS P/N 602184-000	59954	BW	BW		11-94
	B	CHG PN UG, CHG SHTS	60290	BW	BW		2-95
	C	CHG SHTS 1 THRU 20	60813	DP	DP		7-95
	D	CHG SHTS 2, 3, 4, 6, 7	63487	MK	MK		1 07
	G	CHG SHTS 8 THRU 19	73659	SX	SX		12-01

TDM_MAST_OE*
TDM_DAT_LOOP_N
COMB_TDM_OE_A
COMB_TDM_OE_B
COMB_TDM_OE_C
ASIC_TDM_OE
BUS_TDM_DAT*[23-0]
TX_TDM_DAT[23-0]
RX_TDM_DAT_CMOS[23-0]
RX_TDM_DAT_TTL[23-0]
RX_TDM_START_TTL
RX_TDM_CLK_D1V2
TDM_DAT_CLK_A
TDM_DAT_CLK_B
TDM_PH0_A
TDM_PH1_A
TDM_PH1_B

TDM MIXER ASIC U6
TDM_PH0, TDM_PH1, TDM_START, TDM_OE
DAT_IN<23:0>, DAT_OUT<23:0>

74FCT573C U1, U2, U3, U4
74FCT573C

CY7B992 U5 PROGRAMMABLE SKEW CLK BFR
FB, FS, TEST, 4F1, 4F0, 3F1, 3F0, 2F1, 2F0, 1F1, 1F0
4Q1, 4Q0, 3Q1, 3Q0, 2Q1, 2Q0, 1Q1, 1Q0, REF

74FB2033 U7, U8, U9
1MODE1, 1MODE0, 0MODE1, 0MODE0, OEA, OEB, OEB*, LOOPBACK, CLKAB/LEAB, CLKBA/LEBA
B8*, B7*, B6*, B5*, B4*, B3*, B2*, B1*
A18, A17, A16, A15, A14, A13, A12, A11
A08, A07, A06, A05, A04, A03, A02, A01

TP1, TP2, TP3, TP4, TP5, TP8, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36

R1 100, R2 4.7K, R3 100, R4 100, R5 4.7K, R6 4.7K, R7 4.7K, R8 4.7K, R9 100, R10 100, R11 4.7K, R12 4.7K, R58 0, R59 0, R60 0

Vcc, DGND, DGNC

CAD GENERATED DRAWING	ADAM	90307510	
FILENAME: "schematics/902775 10/d	MODEL	NEXT ASS'Y	

DR BW	CK	APP	
DATE 01 14 94			
TELEX® TELEX COMMUNICATIONS, INC. MINNEAPOLIS, MINNESOTA			
TITLE: ANALOG I/O CARD TDM BUS			
SIZE D	DWG. NO. 902775 0	SHT. 1 OF 20	

LN 8E

SHEET	SHEET REVISION STATUS
REV.	

REVISIONS

LOC	REV.	DESCRIPTION	ECO NO	DRFT	CHKR	APP	DATE
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	ADDED TEST POINTS	63787	MK	MK		4-97

BUS_TDM_DAT*[23-0]
BUS_TDM_START*
BUS_1X_CLK*
BUS_256X_CLK*
ARB_BUSA_EN_L
ARB_BUSB_EN_L

U10
ARB_A_REQ_OUT_L
ARB_A_DAT_OUT
ARB_A_BUSY_OUT
TP40
TP39
TP38
74ABT125

U11
ARB_B_REQ_OUT_L
ARB_B_DAT_OUT
ARB_B_BUSY_OUT
BUSB_ARB_REQ_L
BUSB_ARB_DAT
BUSB_ARB_BUSY_L
74ABT125

U12
SRC_A_TALK_EN_L
MPU_TALK_DAT
MPU_TALK_CLK
DEST_A_TALK_EN_L
BUSA_MSG_DAT
BUSA_MSG_BUSA_MSG_CLK
BUSA_ACK_DAT
BUSA_ACK_CLK
TP63
TP64
TP65
TP60
TP61
TP62
74ABT125

U13
SRC_B_TALK_EN_L
DEST_B_TALK_EN_L
BUSB_MSG_DAT
BUSB_MSG_CLK
BUSB_ACK_DAT
BUSB_ACK_CLK
74ABT125

U14
BUSA_ARB_REQ_L
BUSA_ARB_DAT
BUSA_ARB_BUSY_L
TP46
TP45
TP44
74ABT125

U15
BUSB_ARB_REQ_L
BUSB_ARB_DAT
BUSB_ARB_BUSY_L
74ABT125

U16
BUSA_ACK_DAT
BUSA_ACK_CLK
BUSA_MSG_DAT
BUSA_MSG_CLK
74ABT125

U17
BUSB_ACK_DAT
BUSB_ACK_CLK
BUSB_MSG_DAT
BUSB_MSG_CLK
74ABT125

Vcc
R62
10K
R61
10K

J1
CON_VCC
CON_-15V
CON_+15V
AGND
DGND
BUS_TDM_DAT*[16]
BUS_TDM_DAT*[17]
BUS_TDM_DAT*[22]
BUS_TDM_DAT*[15]
BUS_TDM_DAT*[6]
BUS_TDM_DAT*[7]
BUS_TDM_DAT*[18]
BUS_TDM_DAT*[19]
BUS_TDM_DAT*[5]
BUS_TDM_DAT*[2]
BUS_TDM_DAT*[4]
BUS_TDM_DAT*[5]
BUS_TDM_DAT*[20]
BUS_TDM_DAT*[21]
BUS_TDM_DAT*[9]
BUS_TDM_DAT*[23]
BUSA_ARB_REQ_L
BUSA_MSG_CLK
BUSA_ARB_DAT
BUSA_MSG_DAT
BUSA_ARB_BUSY_L
BUSB_MSG_CLK
BUSB_ARB_REQ_L
BUSB_MSG_DAT
BUSB_ARB_DAT
BUSA_ACK_CLK
BUSB_ARB_BUSY_L
BUSA_ACK_DAT
BUSB_ACK_CLK
BUS_TDM_DAT*[1]
BUS_TDM_DAT*[0]
BUS_TDM_DAT*[10]
BUS_TDM_DAT*[11]
BUS_TDM_DAT*[14]
BUS_TDM_DAT*[8]
CARD_ID[0]
CARD_ID[1]
CARD_ID[2]
CARD_ID[4-0]
BUS_TDM_DAT*[3]
BUS_TDM_DAT*[2]

RX_TDM_CLK_DIV2
SRC_LISTEN_A_EN_L
DEST_LISTEN_A_EN_L
SRC_LISTEN_B_EN_L
DEST_LISTEN_B_EN_L
CARD_ID[4-0]
TP66
TP67
ARB_REQ_IN_L
ARB_DAT_IN
ARB_BUSY_IN_L
MPU_LISTEN_DAT
MPU_LISTEN_CLK

TX_TDM_CLK_DIV2_1_2
TX_TDM_CLK_DIV2_3_4
TX_TDM_CLK_DIV2_5_6
TX_TDM_CLK_DIV2_7_8
TX_TDM_CLK_DIV2_9
TX_TDM_CLK_D_V2_10_11
TX_TDM_CLK_D_V2_12_13
TX_TDM_CLK_DIV2_14_15
TX_TDM_CLK_DIV2_16_17

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

DR	CK	APP	TITLE
DATE 8/8			ANALOG I/C CARD BACKPLANE I/O

TELEX COMMUNICATIONS, INC
MINNEAPOLIS, MINNESOTA

ADAM	90307510
MODEL	NEXT ASS'Y

SIZE D | DWG NO. 90277510 | SHT 2 OF ___

BE LS

SHEET REV.	SHEET REVISION STATUS

REVISIONS							
LOC	REV.	DESCRIPTION	ECC NO	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG PN C81,C171;CONNECT U28	60290	BW	BW		2-95
	C	REVISED PER ECO	62813	DP	DP		7-95
	D	ADDED RESET_BG	63457	MK	MK		4-97

RESET_H
DS1
Q1 MMBTA13
R47 10K
Vcc
X001
R13
RESET
SW1
C81 .47uF/35V
U28 HC14
DGND
C80 22pF/50V
R14 100
X4 16.000MHz
C79 22pF/50V
R5 100K
U18 80C196NT
XTAL1
RESET*
EA*
NMI
BHE_W
READY
XTAL2
WRH*
SLP_INT
RD*
WR*
INST
ALATCH*
TP10
TP11
TP12
TP13
MPU_RD_STB*
MPU_WR_STB
MPU_ADDR_LATCH*
LEDS_INSTALLED
MPU_ADDR[19..0]
MPU_DAT[7..0]
A_CH7
A_CH6
A_CH5
A_CH4
ADDR<19>
ADDR<18>
ADDR< 17>
ADDR< 16>
EXT PORT
PORT0
PORT4
PORT3
PORT1
PORT6
PORT2
EPA7
EPA6
EPA5
EPA4
EPA3
EPA2
EPA1
EPA0
ADDR/DATA<7>
ADDR/DATA<6>
ADDR/DATA<5>
ADDR/DATA<4>
ADDR/DATA<3>
ADDR/DATA<2>
ADDR/DATA<1>
ADDR/DATA<0>
ADDR<15>
ADDR<14>
ADDR<13>
ADDR<12>
ADDR<11>
ADDR<10>
ADDR<9>
ADDR<8>
TP37
XLNX_PROG_CLK
XLNX_PROG_DAT
XLNX_PROG_DONE
RX_IX_CLK
ASIC_BUSY
TP9
BSCAN_RETURN
CLIP_INT_L
RX_485_DATA
TI_CIR
TI_CLK
EPA9
EPA8
HDLDx
EXT_INT
RXD
SDI
SCI
SDO
SCO
CLKOUT
HLDAx
INTOUTx
BREQx
TXD
VPP
VREF
AN_GND
VCC
VSS
L78
C172 1.0uF/35V
C78 .10uF/50V
MPU_L_STEN_CLK
MPU_L_STEN_DAT
R35 10K
R51 10K
ASIC_ARES_L
U29
EN
EN*
MPU_ADDR(19)
MPU_ADDR(18)
MPU_ADDR(17)
FCT139
UPPER_HALF_MEG_L
LOWER_HALF_MEG_L
R49 0
R50 0
RAM_CS_L
MPU_RD_STB*
MPU_WR_STB*
U19
U22
MS621008
CS*
R/W*
OE*
R16 100K
R17 100K
ADDR<16>
ADDR<15>
ADDR<14>
ADDR<13>
ADDR<12>
ADDR<11>
ADDR<10>
ADDR<9>
ADDR<8>
ADDR<7>
ADDR<6>
ADDR<5>
ADDR<4>
ADDR<3>
ADDR<2>
ADDR<1>
ADDR<0>
DATA<7>
DATA<6>
DATA<5>
DATA<4>
DATA<3>
DATA<2>
DATA<1>
DATA<0>
U21 CHIP TO BE INSTALLED TO PC BOARD
UTILIZING STANDARD IC SOCKET
TELEX P/N ?
U21
U20
74HC573C
LATCH*
TP14
TP15
MPU_TALK_DAT
MPU_TALK_CLK
BSCAN_CLK
BSCAN_CONF
BSCAN_SEND
RS485_TX_H_RX_L
TX_485_DATA
ARES_L

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

ADAM	90307510	
MODEL	NEXT ASSY	

DR BW	CK	APP	
DATE 011494			

TITLE: ANALOG I/O CARD PROCESSOR SECTION

TELEX COMMUNICATIONS, INC. MINNEAPOLIS, MINNESOTA

SIZE D | DWG NO 90277510 | SHT 3 OF

BE LN

SHEET	SHEET REVISION STATUS
REV.	

REVISIONS						
LOC.	REV.	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-9
	B	CHG PN U6,7-9&1 WAS TP51	60290	BW	BW		2-95

U6
TDM MIXER ASIC

TP17

ASIC_SER_IN_CLK 126 CL_SER_IN_CLK
ASIC_SER_OUT_CLK 1 6 CL_SER_OUT_CLK

ASIC_TALK_CH_6_7 SER_IN<7> SER_OUT<7> 18
SER_IN<6> SER_OUT<6> 19 ASIC_LISTEN_CH_6_7
ASIC_TALK_CH_4_5 SER_IN<5> SER_OUT<5> 20
SER_IN<4> SER_OUT<4> 21 ASIC_LISTEN_CH_4_5
ASIC_TALK_CH_2_3 SER_IN<3> SER_OUT<3> 60
SER_IN<2> SER_OUT<2> 2 ASIC_LISTEN_CH_2_3
ASIC_TALK_CH_0_1 SER_IN<1> SER_OUT<1> 3 ASIC_LISTEN_CH_0_1
SER_IN<0> SER_OUT<0>

TP6 DGND TP7

5,7 MPU_DATA[7-0] MPU_DATA[7-0]

U6
TDM MIXER ASIC

TP 8

ASIC_CS_L 38 CONTR_CS*
ASIC_STB_L 39 CONTR_STB*

TP19

CONTR_DAT<7> 27 MPU_DATA[7]
CONTR_DAT<6> 29 MPU_DATA[6]
CONTR_DAT<5> 30 MPU_DATA[5]
CONTR_DAT<4> 31 MPU_DATA[4]
CONTR_DAT<3> 33 MPU_DATA[3]
CONTR_DAT<2> 35 MPU_DATA[2]
CONTR_DAT<1> 36 MPU_DATA[1]
CONTR_DAT<0> 37 MPU_DATA[0]

ASIC_ARES_L 8 RESET* BUSY 88 ASIC_BUSY 3
TIMER_INT* 90
OVFL_INT* 92 ASIC_OVFL_L 7

TP20 TP21

TP53 TP52 TP51

PAR_AUD_HI_EN_L
PAR_AUD_MD_EN_L
PAR_AUD_LO_EN_L

PAR_CAPTURE
PAR_AUC_RD_H_WR_L

TP50 TP61

Vcc

U30
74HC646

OE* 21
DIR_AB_H_BA_L 3
REG_AB 2
CAB 1
REG_BA 22
CBA 23

A7 11 B7 13 MPU_DATA[7]
A6 10 B6 14 MPU_DATA[6]
A5 9 B5 15 MPU_DATA[5]
A4 8 B4 16 MPU_DATA[4]
A3 7 B3 17 MPU_DATA[3]
A2 6 B2 18 MPU_DATA[2]
A1 5 B1 19 MPU_DATA[1]
A0 4 B0 20 MPU_DATA[0]

U5
TDM MIXER ASIC

ASIC_PAR_CS_L 61 CL_CS*
ASIC_PAR_WR_L 60 CL_WR*
ASIC_PAR_RD_L 59 CL_RD*

TP49 TP48 TP47

CL_PAR_DAT<23> 80
CL_PAR_DAT<22> 78
CL_PAR_DAT<21> 77
CL_PAR_DAT<20> 76
CL_PAR_DAT<19> 74
CL_PAR_DAT<18> 73
CL_PAR_DAT<17> 72
CL_PAR_DAT<16> 71
CL_PAR_DAT<15> 69
CL_PAR_DAT<14> 68
CL_PAR_DAT<13> 66
CL_PAR_DAT<12> 64
CL_PAR_DAT<11> 63
CL_PAR_DAT<10> 57
CL_PAR_DAT<9> 56
CL_PAR_DAT<8> 54
CL_PAR_DAT<7> 52
CL_PAR_DAT<6> 51
CL_PAR_DAT<5> 49
CL_PAR_DAT<4> 48
CL_PAR_DAT<3> 46
CL_PAR_DAT<2> 44
CL_PAR_DAT<1> 43
CL_PAR_DAT<0> 41 40

Vcc

U31
74HC646

OE* 21
DIR_AB_H_BA_L 3
REG_AB 2
CAB 1
REG_BA 22
CBA 23

A7 11 B7 13 MPU_DATA[7]
A6 10 B6 14 MPU_DATA[6]
A5 9 B5 15 MPU_DATA[5]
A4 8 B4 16 MPU_DATA[4]
A3 7 B3 17 MPU_DATA[3]
A2 6 B2 18 MPU_DATA[2]
A1 5 B1 19 MPU_DATA[1]
A0 4 B0 20 MPU_DATA[0]

PAR_AUD_HI_WR_CLK
PAR_AUD_MD_WR_CLK
PAR_AUD_LO_WR_CLK

TP54 TP55 TP56

Vcc

U32
74HC646

OE* 21
DIR_AB_H_BA_L 3
REG_AB 2
CAB 1
REG_BA 22
CBA 23

A7 11 B7 13 MPU_DATA[7]
A6 10 B6 14 MPU_DATA[6]
A5 9 B5 15 MPU_DATA[5]
A4 8 B4 16 MPU_DATA[4]
A3 7 B3 17 MPU_DATA[3]
A2 6 B2 18 MPU_DATA[2]
A1 5 B1 19 MPU_DATA[1]
A0 4 B0 20 MPU_DATA[0]

TP16

Vcc

R18 4.7K
R19 4.7K
R20 4.7K

U5
TDM MIXER ASIC

ASIC_ARES_L R44 0 BSCAN_RES*
BSCAN_CONF R43 0 BSCAN_CONF_DAT
BSCAN_CLK R42 0 BSCAN_CLK
BSCAN_SEND 0 BSCAN_SDAT_IN
BSCAN_SDAT_OUT 87 BSCAN_RETURN 3

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

DR	CK	APP	TITLE
BW			ANALOG I/O CARD
DATE 8 1404			TDM ASIC PORTS

TELEX®
TELEX COMMUNICATIONS, INC.
MINNEAPOLIS, MINNESOTA

ACAD	9030751Ø
MDEL	NEXT ASS'Y

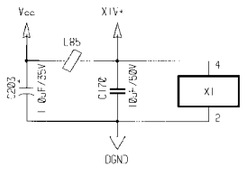
SIZE D DWG NO 90277510 SH 2 OF

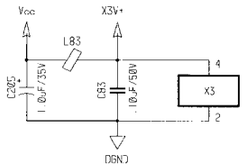
BE LN

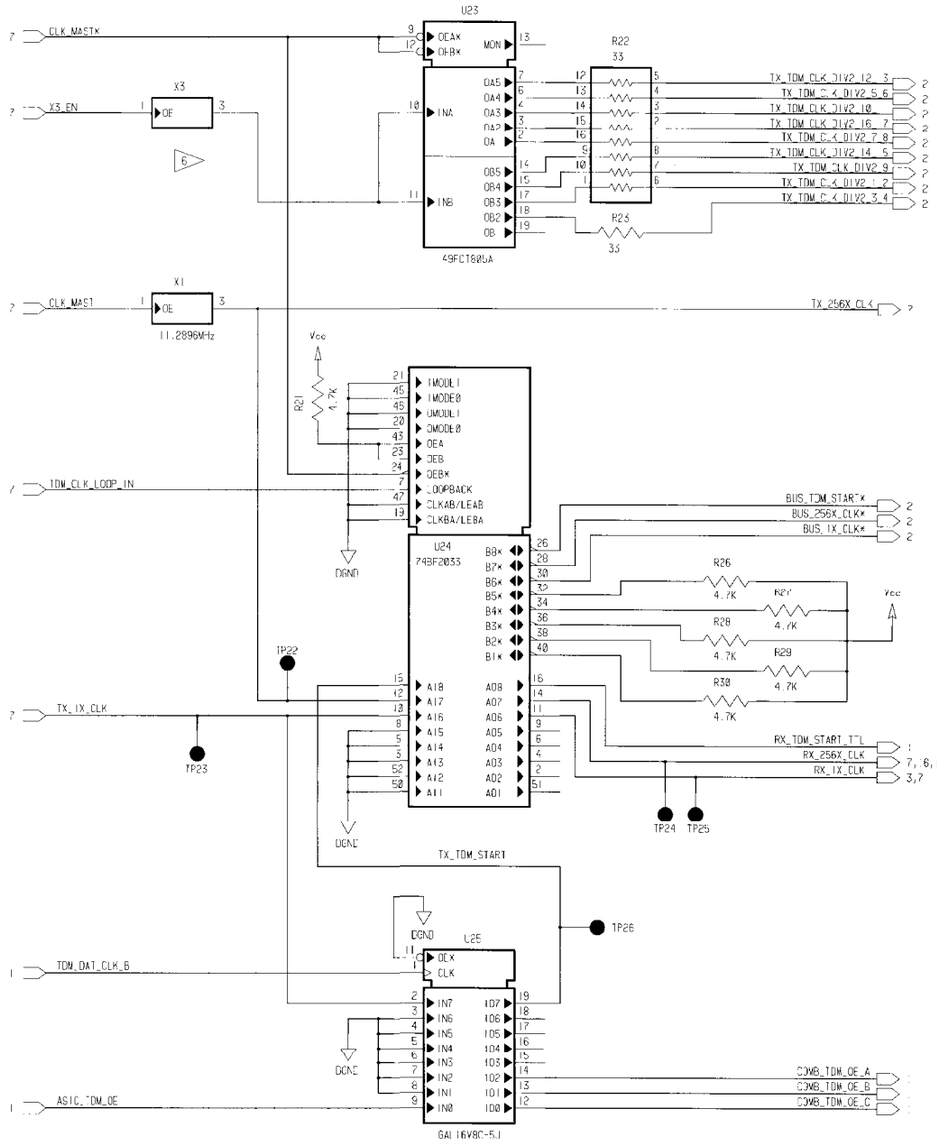
6 ADAM OS (5000) USES 15.00MHZ ADAM (6000) USES 22.4MHZ

REVISIONS						
DOC.	REV	DESCRIPTION	ECO NO.	DRFT	CHKR	APP DATE
	A	RELEASE	59954	BW	BW	1-94
	B	R22 WAS 680 OHMS	60290	BW	BW	2-95
	C	X2,R25,R24 DELETED	60813	DP	DP	7 95

SHEET REV | SHEET REVISION STATUS







CAD GENERATED DRAWING
FILENAME: SEE SHT 1

DR BW	CK	APP	TITLE: ANALOG I/O CARD CLOCK MODULE
DATE 2/11/94			
ADAM	90307510		TELEX COMMUNICATIONS, INC. MINNEAPOLIS, MINNESOTA
MODEL	NEXT ASSY		SIZE D DWG. NO 90277510 SHT 5 OF

BR LN

SHEET	SHEET REVISION STATUS
REV.	

REVISIONS							
LOC.	REV.	DESCRIPTION	ECN NO	DRFT	CHKR	APP	DATE
	A	RELEASE	58954	BK	BW		11-94
	B	CHG PIN J2	60250	BK	BW		2-95

+15V

J2

I/O CONNECTOR

TO_CHN1_AUD_HIGH 8
TO_CHN2_AUD_HIGH 9
TO_CHN3_AUD_HIGH 10
TO_CHN4_AUD_HIGH 11
TO_CHN5_AUD_HIGH 12
TO_CHN6_AUD_HIGH 13
TO_CHN7_AUD_HIGH 14
TO_CHN8_AUD_HIGH 15

TO_CHN1_AUD_LOW 8
TO_CHN2_AUD_LOW 9
TO_CHN3_AUD_LOW 10
TO_CHN4_AUD_LOW 11
TO_CHN5_AUD_LOW 12
TO_CHN6_AUD_LOW 13
TO_CHN7_AUD_LOW 14
TO_CHN8_AUD_LOW 15

FROM_CHN8_AUD_LOW 15
FROM_CHN7_AUD_LOW 14
FROM_CHN6_AUD_LOW 13
FROM_CHN5_AUD_LOW 12
FROM_CHN4_AUD_LOW 11
FROM_CHN3_AUD_LOW 10
FROM_CHN2_AUD_LOW 9
FROM_CHN1_AUD_LOW 8

FROM_CHN8_AUD_HIGH 15
FROM_CHN7_AUD_HIGH 14
FROM_CHN6_AUD_HIGH 13
FROM_CHN5_AUD_HIGH 12
FROM_CHN4_AUD_HIGH 11
FROM_CHN3_AUD_HIGH 10
FROM_CHN2_AUD_HIGH 9
FROM_CHN1_AUD_HIGH 8

-15V

AGND DGND

Vcc

C82 .1UF/50V

DGND

R31 1K

U26

RS485_TX_L_RX_L 3
TX_485_DATA 3

TX_EN 3
RX_EN 2
BUS_D 6
BUS_D* 7
TX_D 4
RX_D 1

751768

U26 CHIP TO BE INSTALLED TO PC BOARD
UTILIZING STANDARD DIP IC SOCKET
TELEX P/N 53041-002

R34 1Ω

R32 1Ω

R33 1K

R48 10K

RX_485_DATA 3

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

DR	BW	CK	APP
DATE	07/1494		

TITLE
ANALOG I/O CARD
CABLE I/O

TELEX®
TELEX COMMUNICATIONS, INC.
MINNEAPOLIS, MINNESOTA

MODEL	NEXT ASSY
ADAM 90307510	

SIZE	DWG NO
D	90277510

SHT 6 OF

SHEET	SHEET REVISION STATUS
REV.	

REVISIONS

LOC	REV.	DESCRIPTION	ECO NO	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BN	BN		11-94
	B	CHG U27 (CONNEC" PWR PINS)	60290	BN	BN		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	ADDED U33	63987	MK	MK		4-97

J4

R36 0

R37 1K

R46 1K

R38 0

R39 0

R40 0

U27 XC3090A

DONE/PGM, LDC, HDC, DOUT

INIT, ARES_L, DIN, CCLK, PWRDWNK, CLK

XLNK_PROG_DONE, ARES, XLNK_PROG_DAT, XLNK_PROG_CLK

RX_256X_CLK

RX_1X_CLK, TALK_CH_1_2, TALK_CH_3_4, TALK_CH_5_6, TALK_CH_7_8

CARD_ID[4], CARD_ID[3], CARD_ID[2], CARD_ID[1], CARD_ID[0]

CARD_ID[4-0] CARD_ID[4-0]

MPU_ADDR[19-0]

MPU_ADDR[19], [18], [17], [16], [15], [14], [4], [3], [2], [1], [0]

MPU_DAT[7], [6], [5], [4], [3], [2], [1], [0]

MPU_WR_STB*, MPU_RD_STB*, ARB_REQ_IN_L, ARB_DAT_IN, ARB_BUSY_IN_L

TX_256X_CLK

ASIC_LISTEN_CH_6_7, ASIC_LISTEN_CH_4_5, ASIC_LISTEN_CH_2_3, ASIC_LISTEN_CH_0_1

ASIC_OVFL_L

TP27 TP28

CLIP_INT_L, ASIC_SER_OUT_CLK, ASIC_SER_IN_CLK, CONV_SER_SYNC, CONV_SER_CLK, VOL_SER_DAT, VOL_SER_CLK, SRC_A_TALK_EN_L, DEST_A_TALK_EN_L, ARB_BUSA_EN_L, ARB_BUSB_EN_L, SRC_LISTEN_A_EN_L, SRC_LISTEN_B_EN_L, DEST_LISTEN_A_EN_L, DEST_LISTEN_B_EN_L

ASIC_CS_L, ASIC_STB_L

LED_CLK_5, LED_CLK_4, LED_CLK_3, LED_CLK_2, LED_CLK_1, LED_CLK_0

MUTE_L[7], [6], [5], [4], [3], [2], [1], [0]

VOL_EN[7], [6], [5], [4], [3], [2], [1], [0]

ARB_A_REQ_OUT_BG_L, ARB_A_DAT_OUT_BG, ARB_A_BUSY_OUT_BG_L

CLK_MAST, CLK_MAST*, X3_EN

TX_1X_CLK, TDM_MAST_DEN, TDM_CLK_LOOP_IN, TDM_DAT_LOOP_IN

LISTEN_CH_7_8, LISTEN_CH_5_6, LISTEN_CH_3_4, LISTEN_CH_1_2

ASIC_TALK_CH_0_1, ASIC_TALK_CH_2_3, ASIC_TALK_CH_4_5, ASIC_TALK_CH_6_7

AP_SER_CLK1, AP_SER_CLK2, IO_AP_SER_DAT

ASIC_PAR_CS_L, ASIC_PAR_RD_L, ASIC_PAR_WR_L, PAR_AUD_HI_WR_CLK, PAR_AUD_HI_EN_L, PAR_AUD_LO_WR_CLK, PAR_AUD_LO_EN_L, PAR_AUD_MD_WR_CLK, PAR_AUD_MD_EN_L, PAR_AUD_RD_H_WR_L, PAR_CAPTURE

SRC_B_TALK_EN_L, DEST_B_TALK_EN_L, ARB_B_REQ_OUT_L, ARB_B_DAT_OUT, ARB_B_BUSY_OUT_L

FROM_AP_SER_DAT

R41 1K

LECS_INSTALLED, SOFT_BUTTON

J3

MPU_DAT[7-0]

R52 10K, R25 10K, R24 10K

ARB_A_BUSY_OUT_BG_L, ARB_A_DAT_OUT_BG, ARB_A_REQ_OUT_BG_L

U33 F32

ARB_A_REQ_OUT_L, ARB_A_DAT_OUT, ARB_A_BUSY_OUT_L

RESET_H

J5

DGND

MPU_DAT[7-0]

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

DR	DN	CK	APP
DATE	011494		

TELEX
TELEX COMMUNICATIONS, INC
MINNEAPOLIS, MINNESOTA

TITLE: ANALOG I/O CARD
X1_INX

ADAM	90307510
MODE	NEXT ASS'Y

SIZE D

DWG NO 90277510

SHT 7 OF

BE LN

SHEET REV.	SHEET REVISION STATUS

REVISIONS							
LOC	REV	DESCRIPTION	ECO NO	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG R100-101,C125-126,U101,C117,R105	60290	BW	BW		2-95
	C	REVISED PER ECO	608 3	DP	DP		7-95
	D	CHNG P/N; R106	73659	SX	SX		12-01

7,9,10,11,12,13,14,15 VO_SER_DAT
7,9,10,11,12,13,14,15 VO_SER_CLK
7 VO_ENL0J
7 MUTE_LL0J
16 TO_CHN1_AUD
6 FROM_CHN1_AUD_HIGH
6 FROM_CHN1_AUD_LOW

R118 1.5K DGND

C101 33pF/50V
R100 182K
R104 20K
R119 22.1K
R121 182K
U100 TL072
LINE RECEIVER
C100 33pF/50V AGND
R103 19.6K
R102 1K CMRR ADJUST AGND

TP100
TP101
TP102

U103 CS3310 GAIN CONTROL
SCDATAO SCDATAI SCK _CS _MUTE ZCEN VD- DGND VA+ VA- AINL AGNDL AINR AGNDR AOUTL AOUTR

C110 10uF/25V DGND
C111 .10uF/50V DGND
R114 10
+5V ANALOG, CHN 1,2
-5V ANALOG, CHN 1,2
C112 10uF/25V AGND
C113 .10uF/50V AGND
C114 .10uF/50V
C115 .10uF/50V AGND
AS2/JF101 5.1Ω AGND

C117 22pF/50V
R106 56K
R105 10K
U104 TL072
AGND
R111 562
R107 10K
R108 10K
U104 TL072
AGND
R109 562

C102 .10uF/50V +15V AGND
C103 .10uF/50V -15V AGND

C118 .10uF/50V +15V AGND
C119 .10uF/50V -15V AGND

C121 33pF/50V
U105 NE5534A
+15V -15V
C122 .10uF/50V AGND
R110 6.81K
C120 2200pF/50V
C123 33pF/50V
U 06 NE5534A
+15V -15V
C124 .10uF/50V AGND
LINE DRIVER

R112 30.1
R113 30.1
TP 03
TP104
TO_CHN1_AUD_H GH 6
TO_CHN1_AUD_LOW 6
D100 IN4148
D102 IN4148
D101 IN4148
D103 IN4148
+.5V
-15V

+5V ANALOG, CHN 1,2
+15V
U101 LT1117 ADJ
Vout
C125 33uF/25V
C104 10uF/25V
C105 10uF/50V
C106 .01uF/50V
TP105
AGND

-5V ANALOG, CHN 1,2
-15V
79L05 U102 GND VIN VOUT
C126 33uF/25V
C107 .10uF/50V
AS2/JF101 (+ 8010)
C109 .01uF/50V
AGND

FROM_CHN1_AUD 16

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

DR	CK	APP
BW		

DATE 2/11/97
TCLCX®
TCLEX COMMUNICATIONS, INC.
MINNEAPOLIS, MINNESOTA

TITLE
SCHEMATIC
ANALOG I/O CARD
CHANNEL 1
LINE DRIVER/RECEIVER

ADAM 90307510
MODEL NEXT ASSY

SIZE D
DWG NO. 90277510
SHT 8 OF

BE LN

SHEET REV	SHEET REVISION STATUS

REVISIONS							
LEC.	REV.	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG R200,R201,R206,C217	60280	BW	BW		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	CHG. R206 WAS: 49.9K	73659	KS	KS	KS	12-01

7,8,10,11,12,13,14,15 VOL_SER_DAT
7,8,10,11,12,13,14,15 VOL_SER_CLK
7 VOL_ENBL
7 MUTE_L
16 TO_CHN2_AUD
R218 1.5K
DGND
TP200
C201 33pF/50V
R202 182K
R204 20K
6 FROM_CHN2_AUD_HIGH
R219 22.1K
6 FROM_CHN2_AUD_LOW
R201 182K
U100 TL072
LINE RECEIVER
TP201
C200 33pF/50V
R203 19.6K
R202 1K CMRR ADJUST
AGND
C210 10uF/25V
C211 .10uF/50V
DGND
R214 10
+5V ANALOG, CHN 1,2
U203 CS3310
SDATAO SDATAI SCK _CS _MUTE ZCEN
VD+ DGND VA+ VA-
AINL AGNDL AINR AGNDR
AOUTL ACUTR
GAIN CONTROL
TP202
C212 0.47/25V
C213 .10uF/50V
C214 .10uF/50V
C215 .10uF/50V
C216 ASZ/10V
C217 22pF/50V
R205 56K
R205 10K
U204 TL072
R207 10K
R208 10K
R209 562
R210 6.81K
R211 562
C220 2200pF/50V
C221 33pF/50V
U205 NE5534A
R212 30.1
TP203
TO_CHN2_AUD_HIGH 6
C222 10uF/50V
+15V
-15V
D200 1N4148
D203 1N4148
D201 1N4148
D202 1N4148
U206 NE5534A
R213 30.1
TO_CHN2_AUD_LOW 6
TP204
C223 33pF/50V
C224 10uF/50V
C218 .10uF/50V
C219 .10uF/50V
LINE DRIVER
FROM_CHN2_AUD 16

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

ADAM	903075Ø
MODEL	NEXT ASSY

DR BW	CK	APP
DATE 011494		

TELEX®
TELEX COMMUNICATIONS, INC.
MINNEAPOLIS, MINNESOTA

TITLE
SCHEMATIC
ANALOG I/O CARD
CHANNEL 2
LINE DRIVER/RECEIVER

SIZE D | DWG NO. 80277510 | SHT 9 OF

BE LS

SHEET REV.	SHEET REVISION STATUS

REVISIONS

LOC.	REV.	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG R300 1,C325-6,U301,C317,R306	60290	BW	BW		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	CHG. R306 WAS: 49.9K	73659	KS	KS	KS	12-01

+5V ANALOG, CHN 3,4

-5V ANALOG, CHN 3,4

7,8,9,11,12,13,14,15 VOL_SER_DAT

7,8,9,11,12,13,14,15 VOL_SER_CLK

7 VOL_EN(2)

7 MUTE_L(2)

17 TO_CHN3_AUD

R314 10

C310 10uF/25V

C311 .10uF/50V

C312 10uF/25V

C313 .10uF/50V

C314 10uF/50V

C315 .10uF/50V

C316 .022uF/50V

U303 CS3310

SDATAO, SDATAI, SCK, _CS, _MJTE, ZCEN, VD+, DGND, VA+, VA-, AINL, AGNDL, AOUTL, AINR, AGNDR, AOUTR

R318 1.5K

TP300

C301 33pF/50V

R304 20K

R300 192K

R319 22.1K

R301 182K

FROM_CHN3_AUD_HIGH 5

FROM_CHN3_AUD_LOW 6

U300 TL072

LINE RECEIVER

TP301

TP302

C317 22pF/50V

R306 56K

R305 10K

U304 TL072

R311 562

C321 33pF/50V

U305 NE5534A

R312 30.1

TP303

TO_CHN3_AUD_HIGH 6

C320 2200pF/50V

R310 6.31K

C322 .10uF/50V

C323 33pF/50V

U306 NE5534A

R313 30.1

TP304

TO_CHN3_AUD_LOW 6

D300 1N4148

D303 1N4148

D301 1N4148

D302 1N4148

R307 10K

R308 10K

R309 562

U304 TL072

C318 10uF/50V

C319 .10uF/50V

C324 .10uF/50V

LINE DRIVER

FROM_CHN3_AUD 17

C330 33pF/50V

R303 19.6K

R302 1K CMRR ADJUST

C302 .10uF/50V

C303 .10uF/50V

+15V

-15V

AGND

DGND

+5V ANALOG, CHN 3,4

-15V

U301 LT1117 ADJ

C325 33uF/25V

C304 10uF/25V

C305 .10uF/50V

C306 10uF/50V

TP305

-5V ANALOG, CHN 3,4

U302 79L05

C326 33uF/25V

C307 .10uF/50V

C308 .022uF/50V

C309 .10uF/50V

CAD GENERATED DRAWING

FILENAME: SEE SHT 1

DR	CK	APP
BW		

DATE 011494

TELEX®

TELEX COMMUNICATIONS, INC.

MINNEAPOLIS, MINNESOTA

ADAM	90307510
MODEL	NEXT ASSY

TITLE

SCHEMATIC

ANALOG I/O CARD

CHANNEL 3

LINE DRIVER/RECEIVER

SIZE D DWG. NO. 90277510

SHT 10 OF

SHEET REVISION STATUS	SHEET REV.

REVISIONS							
LOC	REV.	DESCRIPTION	ECO NO.	DR'T	CHK'R	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG R400,R401,C4 7,R40E	60290	BW	BW		2-95
	C	REVISED PER ECO	60813	JP	CP		7-95
	D	CHG. R406 WAS: 49.9K	73659	KS	KS	KS	12-01

+5V ANALOG, CHN 3.4

-5V ANALOG, CHN 3.4

7 8,9,10,12,13,14,15 VOL_SER_DAT

7 8,9,10,12,13,14,15 VOL_SER_CLK

7 VOL_ENL3J

7 MUTE L[3J

17 TO_CHN4_AUD

FROM_CHN4_AUD_HIGH 6

FROM_CHN4_AUD_LOW 6

R414 10

C410 10uF/25V

C411 .10uF/50V

C44 10uF/50V

C412 10uF/25V

C413 .10uF/50V

C415 .10uF/50V

C416 ASZ/JF01

DGND

AGND

U403 CS3310

SCATAO VD+

SCATAI DGND

SCK

_CS

_MUTE VA+

ZCEN VA-

AINL AOUTL

AGNDL

AINR AOUTR

AGNDR

GAIN CONTROL

TP400

TP401

TP402

R418 1.5K

C40 33pF/50V

R404 20K

R402 1K CMRR ADJUST

R400 182K

R419 22.1K

R401 182K

U300 TL072

LINE RECEIVER

C400 33pF/50V

R403 19.6K

C417 22pF/50V

R406 56K

R405 10K

U404 TL072

R411 562

R407 0K

R410 13.3K

C420 220pF/50V

R408 10K

R409 562

C418 10uF/50V

C419 .10uF/50V

C421 33pF/50V

U405 NE5534A

C422 .10uF/50V

C423 33pF/50V

U406 NE5534A

C424 10uF/50V

+15V

-15V

R412 30.1

R413 30.1

TP403

TP404

D400 IN4148

D403 IN4148

D401 IN4148

D402 IN4148

TO_CHN4_AUD_HIGH 6

TO_CHN4_AUD_LOW 6

LINE DRIVER

FROM_CHN4_AUD 7

CAD GENERATED DRAWING

FILENAME: SEE SHT 1

DR	CK	APP
BW		

DATE 011494

TELEX®

TELEX COMMUNICATIONS, INC.

MINNEAPOLIS, MINNESOTA

TITLE

SCHEMATIC

ANALOG I/O CARD

CHANNEL 4

LINE DRIVER/RECEIVER

ADAM	90207510
MODEL	NEXT ASS'Y

SIZE D

DWG. NO. 90277510

SHT. 11 OF

BE LN

SHEET REV.	SHEET REVISION STATUS

REVISIONS							
LOC.	REV	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG R500-1,C525-6,U501,C517,R506	60290	BW	BW		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	CHG. R506 WAS: 49.9K	73659	KS	KS	KS	12-01

7,8,9,10,11,13,14,15 VOL_SER_DAT
7,8,9,10,11,13,14,15 VOL_SER_CLK
7 VOL_ENB
7 MUTE_LED
18 TO_CHN5_AUD
6 FROM_CHN5_AUD_HIGH
6 FROM_CHN5_AUD_LOW
18 FROM_CHN5_ALC
6 TO_CHN5_AUD_HIGH
6 TO_CHN5_AUD_LOW

+5V ANALOG, CHN 5,6
-5V ANALOG, CHN 5,6
+15V
-15V
DGND
AGND

U503 GAIN CONTROL
SDATAO, SDATAI, SCK, _CS, _MUTE, ZCEN, AINL, AGNDL, A_NR, AGNDR, VD+, DGND, VA+, VA-, AOUTL, AOUTR, CS3310

U500 TL072 LINE RECEIVER
U504 TL072
U505 NE5534A
U506 NE5534A
U507 TL072 LINE DRIVER

L501 LT1117 ADJ
U502 79L05

R500 182K
R501 182K
R502 1K CMRR ADJUST
R503 19.6K
R504 20K
R505 10K
R506 56K
R507 10K
R508 10K
R509 562
R510 6.81K
R511 562
R512 30.1
R513 30.
R514 10
R518 1.5K
R519 22.1K

C500 33pF/50V
C501 33pF/50V
C502 .10uF/50V
C503 10uF/50V
C504 10uF/25V
C505 .10uF/50V
C506 .10uF/50V
C507 .10uF/50V
C508 .10uF/50V
C509 .10uF/50V
C510 10uF/25V
C511 10uF/50V
C512 10uF/25V
C513 10uF/50V
C514 .10uF/50V
C515 .10uF/50V
C516 10uF/25V
C517 22pF/50V
C518 .10uF/50V
C519 .10uF/50V
C520 2200pF/50V
C521 33pF/50V
C522 10uF/50V
C523 33pF/50V
C524 .10uF/50V
C525 33uF/25V
C526 33uF/25V

D508 IN4148
D509 IN4148
D501 IN4148
D502 IN4148

TP500
TP501
TP502
TP503
TP504
TP505

CAD GENERATED DRAWING
FILLNAME: SEE SHT 1

DR	CK	APP
BW		

DATE 011494

TELEX®
TELEX COMMUNICATIONS, INC.
MINNEAPOLIS, MINNESOTA

MODEL	NEXT ASS'Y
ADAM	90307510

TITLE
SCHEMATIC
ANALOG I/O CARD
CHANNEL 5
LINE DRIVER/RECEIVER

SIZE D DWG. NO. 90277510
SHT 12 OF

BE LN

SHEET REV.	SHEET REVISION STATUS

REVISIONS							
LOC.	REV.	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG R600,R601,R606,C617	60200	BW	BW		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	CHG. R606 WAS: 49.9K	73659	KS	KS	KS	12-01

7,8,9,10,11, 2,14,15 VOL_SER_DAT
7,8,9,10,11, 2,14,15 VOL_SER_CLK
7 VOL_EN(5)
7 MUTE_L(5)
18 TO_CHNG_AUD

+5V ANALOG, CHN 5,6
5V ANALOG, CHN 5,6

R614 10
C610 10uF/25V
C611 .10uF/50V
DGND
C614 .10uF/50V
C612 10uF/25V
C613 .10uF/50V
C615 .10uF/50V
AS27/F01 +9.90
AGND

U603
SDATAO VD+
SDATA DGND
SCK
_CS
_MUTE VA+
ZCEN VA-
AINL AOUTL
AGNDL
AINR AOUTR
AGNDR
CS3310
GAIN CONTROL

R618 5K
TP600
TP601
TP602

C601 33pF/50V
R604 22K
6 FROM_CHNG_AUD_HIGH
R602 182K
R619 22.1K
6 FROM_CHNG_AUD_LOW
R601 182K
U5Ø2 TL072
LINE RECEIVER
C2Ø2 33pF/50V
R603 19.6K
R602 1K CMRR ADJUST

C6.7 22pF/50V
R606 56K
U604 TL072
R605 10K
R607 10K
R61 562
6.8K
C620 2200pF/50V

C621 33pF/50V
U605 NE5534A
C622 .10uF/50V
+15V
-15V
R612 32.1
TP603
TO_CHNG_AUD_HIGH 6
D6Ø3 IN4148
D6Ø4 IN4148

R608 10K
U604 TL072
R609 562
C623 33pF/50V
U606 NE5534A
R613 32.1
TP604
TO_CHNG_AUD_LOW 6
D6Ø1 IN4148
D6Ø2 IN4148
C624 .10uF/50V
C618 .10uF/50V
C619 .10uF/50V
LINE DRIVER

FROM_CHNG_AUD 18

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

DR	CK	APP	TITLE
BW			SCHEMATIC ANALOG I/C CARD CHANNEL 6 LINE DRIVER/RECEIVER
DATE 011494			

TELEX®
TELEX COMMUNICATIONS, INC.
MINNEAPOLIS, MINNESOTA

ACAD	90307510
MODEL	NEXT ASS'Y

SIZE D | DWG. NO. 90277510 | SHT 13 OF ___

BE LN

SHEET	SHEET REVISION STATUS
REV.	

REVISIONS

LOC.	REV.	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		1-94
	B	CHG R700 1, C725 6, U701, C717, R706	60233	DW	DR		2-95
	C	REVISED PER ECO	60913	DP	DP		7-95
	D	CHG. R706 WAS: 49.9K	73659	KS	KS	KS	12-01

+5V ANALOG, CHN 7,8

-5V ANALOG, CHN 7,8

7 8,9,10,11,12,13,15 VOL_SER_DAT

7 8,9,10,11,12,13,15 VOL_SER_CLK

7 VOL_EN(6)

7 MUTE_L(6)

19 TO_CHN7_AUD

R714 10

C710 10uF/25V

C711 .10uF/50V

C714 .10uF/50V

C712 10uF/25V

C713 10uF/50V

C715 10uF/50V

C716 AS2/5F01

DGND

AGND

U703

SDATAO VC+

SDATAI DGND

SCK

_CS

_MUTE VA+

ZCEN VA-

AINL ACUTL

AGNDL

AINR AOUTR

AGNDR CS3310

GAIN CONTROL

TP700

TP701

TP702

R718 7.5K

C721 33pF/50V

R704 20K

R719 22.1K

6 FROM_CHN7_AUD_HIGH

R700 182K

6 FROM_CHN7_AUD_LOW

R701 182K

U700 TL072

LINE RECEIVER

C700 33pF/50V

R703 19.6K

R702 1K

CMRR ADJUST

C702 .10uF/50V

C703 .10uF/50V

+15V

-15V

C717 22pF/50V

R706 56K

R705 10K

U704 TL072

R711 562

R707 10K

R710 6.81K

C720 2200pF/50V

R708 10K

U704 TL072

R709 562

C721 33pF/50V

U705 NE5534A

C722 .10uF/50V

R712 30.1

TP703

TO_CHN7_AUD_HIGH 6

D700 IN4148

D703 IN4148

D701 IN4148

D702 IN4148

C723 33pF/50V

U706 NE5534A

R713 30.1

TO_CHN7_AUD_LOW 6

TP704

C724 .10uF/50V

C718 10uF/50V

C719 .10uF/50V

LINE DRIVER

FROM_CHN7_AUD 19

+5V ANALOG, CHN 7,8

+15V

U701 LT1117 ADJ

C705 .10uF/50V

C706 .10uF/50V

C704 10uF/25V

C725 33uF/25V

TP705

AGND

5V ANALOG, CHN 7,8

-15V

GND

VIN VOUT

79L05 U702

C707 .10uF/50V

C708 10uF/25V

C709 .10uF/50V

C726 33uF/25V

AGND

CAD GENERATED DRAWING

FILENAME: SFF SHT 1

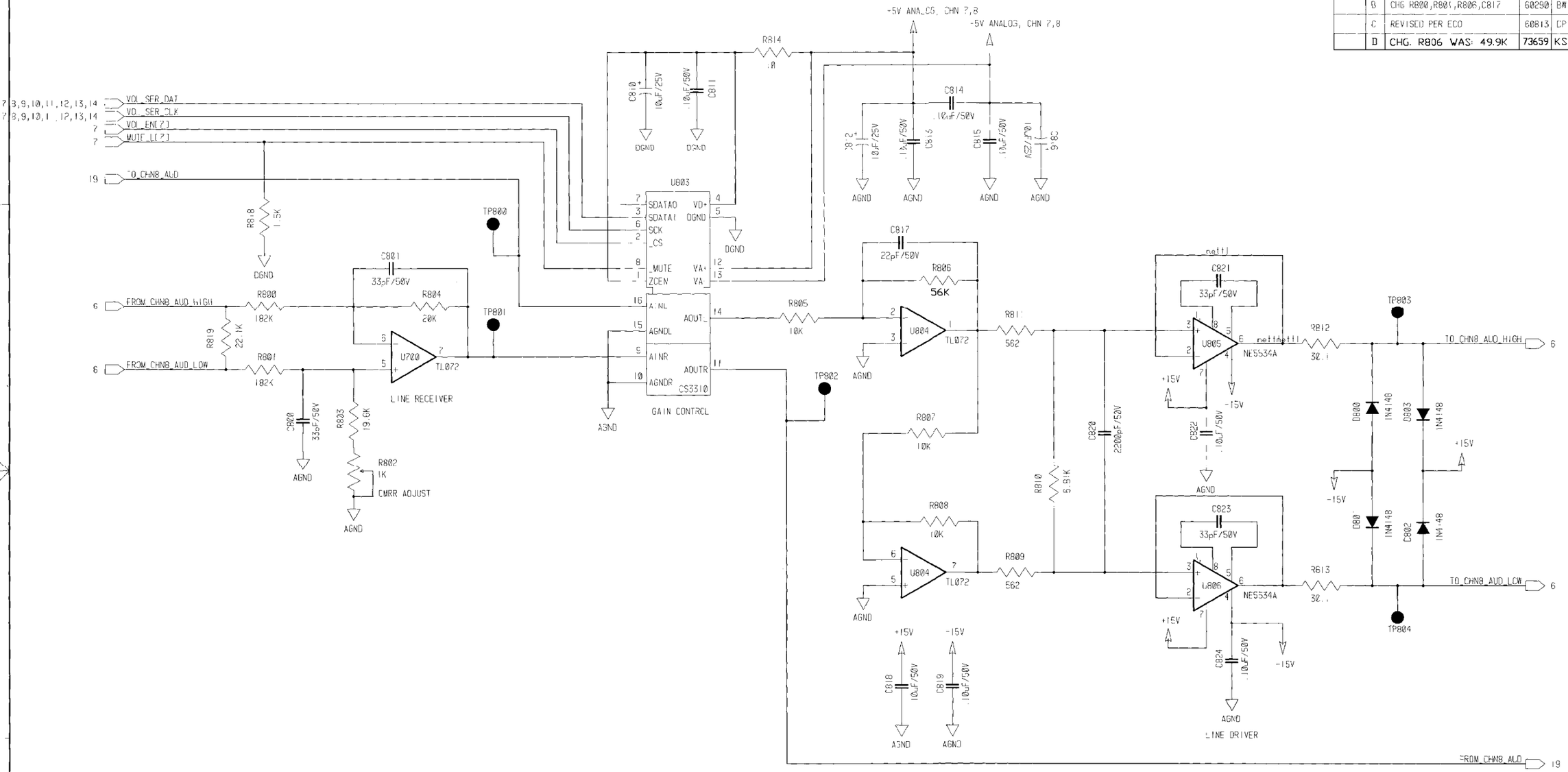
		DR	CK	APP	TITLE
		BW			SCHEMATIC ANALOG I/O CARD CHANNEL 7 LINE DRIVER/RECEIVER
		DATE 011494			
ADAM	90307510	TELEX® TELEX COMMUNICATIONS, INC. MINNEAPOLIS, MINNESOTA			
MODEL	NEXT ASSY	SIZE D	DWG. NO. 90P77510		
			SHT. 14 OF		

BE LN

SHEET REV.	SHEET REVISION STATUS

REVISIONS

LOC.	REV.	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG R800,R801,R806,C817	60290	BW	BW		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	CHG. R806 WAS: 49.9K	73659	KS	KS	KS	12-01



CAD GENERATED DRAWING
FILENAME: SCE SHT 1

ADAM MODEL	9038751Ø NEXT ASSY

DR BW	CK	APP
DATE 011494		

TELEX®
TELEX COMMUNICATIONS, INC.
MINNEAPOLIS, MINNESOTA

TITLE
SCHEMATIC
ANALOG I/O CARD
CHANNEL 8
LINE DRIVER/RECEIVER

SIZE D | DWG. NO. 902775.0 | SHT 15 OF ___

BE LN

SHEET REV.	SHEET REVISION STATUS

REVISIONS							
LOC.	REV.	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG PN C135,C138 SEE ECO	60290	BW	BW		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	CHG. U107 WAS: CS4216; CHG. R121 & R123 WAS: 604	73659	KS	KS	KS	12-01

+5V_CHN1,2

R125 10K

3,7,17,18,19 ARES_L

5,7,17,18,19 RX_256X_CLK

7,17,18, 9 CONV_SER_SYNC

7,17,18, 9 CONV_SER_CLK

7 LISTEN_CH_1_2

U107 CS4218

RESET* 2
PWR_DOWN 13
CLK_IN 3
SER_MODE_3 41
SER_MODE_2 32
SER_MODE_1 29
SER_SYNC 1
SER_CLK 44
MF8 30
MF7 31
MF6 34
MF4 36
MF3 35
C11 33
MF2 39
MF1 40
MF5 38
DO1 37
SDIN 42
SDOUT 43
RIN1 25
RIN2 26
LIN1 27
LIN2 28
ROUT 15
LOUT 16
VD 4
DGND 5
VA 24
AGND 23
REF_BUF 20
REF_BYP 21
REF_GND 22

AGND

C147 22pF/50V

C141 22pF/50V

R127 20K

9 FROM_CHN2_AUD

C144 .47uF/25V

R126 20K

U108 LM833

R115 150

C140 .01uF/25V

C143 .47uF/25V

R128 4.7K

AGND

8 FROM_CHN1_AUD

C145 .47uF/25V

R129 20K

U108 LM833

R30 20K

C142 22pF/50V

R116 AGND 150

C127 .01uF/25V

AGND

+5V_CHN1,2

AGND

C133 .1uF/50V

C134 10uF/25V

AGND

+5V_ANALOG, CHN1,2

U108

C146 .1uF/50V

AGND

Vcc

FB102

+5V_CHN1,2

R117 2

+5V_ANALOG, CHN1,2

C128 47uF/16V

C129 10uF/35V

C150 .1uF/50V

C131 10uF/35V

C132 .1uF/50V

C139 47uF/16V

DGND

AGND

AGND

AGND

TALK_CH_1_2 7

TO_CHN2_AUD 9

R123 0

C138 10uF/35V

C137 2200pF/50V

R124 40.2K

AGND

AGND

TO_CHN1_AUD 8

R121 0

C135 10uF/35V

C136 2200pF/50V

R122 40.2K

AGND

AGND

CAD GENERATED DRAWING

FILENAME: SEE SHT 1

ADAM	90307510
MODEL	NEXT ASSY

DR BW	CK	APP	TITLE
DATE 011494			SCHEMATIC ANALOG I/O CARD CHANNEL 1,2 A/D AND D/A CONVERTER
TELEX® TELEX COMMUNICATIONS, INC. MINNEAPOLIS, MINNESOTA			SIZE D
			DWG. NO 90277510
			SHT 16 OF ___

BF LN

SHEET REV.	SHEET REVISION STATUS

REVISIONS

LTR	REV	DESCRIPTION	ECO NO.	DRN	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG PN C335,C338,SEE ECO	60290	BW	BW		2-95
	C	REVISED PER ECO	60613	DP	DP		7-95
	D	CHG. U307 WAS: CS4216; CHG. R321 & R323 WAS: 604	73659	KS	KS	KS	12-01

+5V_CHN3,4

R325 10K

3,7,16,18,19 ARES_L

5,7,16,18,19 RX_256X_CLK

7,16,18,19 CONV_SER_SYNC

7,16,18,19 CONV_SER_CLK

7 LISTEN_CH_3_4

U307 CS4218

2 RESET×
13 PWR_DWN
3 CLK_IN
41 SER_MODE_3
32 SER_MODE_2
29 SER_MODE_1
1 SER_SYNC
44 SER_CLK
30 MF8
3 MF7
34 MF6
36 MF4
35 MF3
33 D.I
39 MF2
40 MF1
38 MF5
37 DO1
42 SDIN
43 SDOUT
25 RIN1
26 R N2
27 LIN1
28 LIN2
15 ROUT1
16 LOUT1
4 VD
5 DGND
24 VA
23 AGND
20 REF_BUF
21 REF_BYP
22 REF GND

AGND

C341 22pF/50V

R327 20K

11 FROM_CHN4_AUD

C344 .47uF/25V

R326 20K

U308 LM833

R315 150

C340 .01uF/25V

C347 22pF/50V

C343 .47uF/25V

R328 4.7K

10 FROM_CHN3_AUD

C345 .47uF/25V

R329 20K

U308 LM833

R316 150

C327 .01uF/25V

R332 20K

C342 22pF/50V

+5V_ANALOG, CHN3,4

U308

C346 .1uF/50V

AGND

+5V_CHN3,4

AGND

AGND

C333 .1uF/50V

C334 10uF/25V

AGND

TALK_CH_3_4 7

R323 0

C338 10uF/35V

TO_CHN4_AUD 11

C337 2200pF/50V

R324 40.2K

AGND AGND

R321 0

C335 10uF/35V

TO_CHN3_AUD 10

C336 2200pF/50V

R322 40.2K

AGND AGND

Vcc

FB300

+5V_CHN3,4

R317 2

+5V_ANALOG, CHN3,4

C328 47uF/16V

C329 1.0uF/35V

C330 .1uF/50V

C331 1.0uF/35V

C332 .1uF/50V

C339 47uF/16V

DGND

AGND AGND AGND AGND

CAD GENERATED DRAWING

FILENAME: SEE SHT 1

ADAM MODEL	90277510 NEXT ASS'Y

DR	CK	APP
BW		

DATE 011494

TELEX®
TELEX COMMUNICATIONS, INC.
MINNEAPOLIS, MINNESOTA

TITLE
SCHEMATIC
ANALOG I/O CARD
CHANNEL 3,4
A/D AND D/A CONVERTER

SIZE D DWG. NO. 90277510

SHT 12 OF

8 7 6 5 4 3 2 1

B F LN

SHEET	SHEET REVISION STATUS
REV.	

REVISIONS

LOC.	REV	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG PN C535,C538, SEE ECO	60290	BW	BW		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	CHG. U507 WAS: CS4216; CHG. R521 & R523 WAS: 604	73659	KS	KS	KS	12-01

+5V_CHN5,6
R525 10K
3,7,6,17,19 ARES_L
5,7,16,17,19 RX_256X_C_K
7,16,17,19 CONV_SER_SYNC
7,16,17,19 CONV_SER_CLK
7 LISTEN_CH_5_6
U507 CS4218
RESET* PWR_DWN CLK_IN
SER_MODE_3 SER_MODE_2 SER_MODE_1 SER_SYNC SER_CLK
MF8 MF7 MF6 MF4 MF3 DI1
MF2 MF1 MF5 DO1
SDIN SDOUT
RIN1 RIN2 _IN1 _IN2 ROUT LOUT
VD DGND VA AGND REF_BUF REF_BYP REF_GND
C547 22pF/50V
AGND
C541 22pF/50V
R527 20K
13 FROM_CHN6_AUD
C544 .47uF/25V
R526 20K
U508 LM833
R515 150
C540 .010uF/25V
C543 .47uF/25V
R528 4.7K
12 FROM_CHN5_AUD
C545 .47uF/25V
R529 20K
R530 20K
C542 22pF/50V
R516 150
C527 .010uF/25V
+5V_ANALOG, CHN5,6
U508
C546 .10uF/50V
TALK_CH_5_6 7
TO_CHN6_AUD 13
TO_CHN5_AUD 12
R523 0
R521 0
C530 10uF/35V
C535 10uF/35V
C537 2200pF/50V
C536 2200pF/50V
R524 40.2K
R522 40.2K
C533 .10uF/50V
C534 10uF/25V
Vcc
FB500
R517 2
C528 47uF/16V
C529 10uF/35V
C530 .10uF/50V
C531 10uF/35V
C532 .10uF/50V
C539 47uF/16V
DGND
AGND

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

DR	CK	APP	TITLE
BW			SCHEMATIC ANALOG I/O CARD CHANNEL 5,6 A/D AND D/A CONVERTER
DATE 011494			
TELEX® TELEX COMMUNICATIONS, INC. MINNEAPOLIS, MINNESOTA			SIZE D DWG. NO 90277510 SHT 18 OF
ADAM 90307510 MODEL	NEXT ASSY		

BT LN

SHEET REV.	SHEET REVISION STATUS

REVISIONS							
LOC.	REV.	DESCRIPTION	ECO NO.	DRFT	CHKR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG C735,C738, SEE ECO	60290	BW	BW		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95
	D	CHG. U707 WAS: CS4216; CHG. R721 & R723 WAS: 604	73659	KS	KS	KS	12-01

+5V_CHN7,8

R725 10K

3,7,16,17,18 ARES_L

5,7,16,17,18 RX_256X_CLK

7,16,17,18 CONV_SER_SYNC

7,16,17,18 CONV_SER_CLK

7 LISTEN_CH_7_8

U707 CS4218

RESET
PWR_DWN
CLK_IN
SER_MODE_3
SER_MODE_2
SER_MODE_1
SER_SYNC
SER_CLK
MF8
MF7
MF6
MF4
MF3
DI1
MF2
MF1
MF5
DOI
SDIN
SDOUT
RIN1
RIN2
LIN1
LIN2
ROUT
LOUT
VD
DGND
VA
AGND
REF_BUF
REF_BYP
REF_GND

C741 22pF/50V

R57 20K

C747 22pF/50V

AGND

15 FROM CHN8_AUD

C744 .47uF/25V

R726 20K

U708 LM833

R715 150

C740 .010uF/25V

C743 .47uF/25V

R728 4.7K

14 FROM_CHN7_AUD

C745 .47uF/25V

R729 20K

R730 20K

C742 22pF/50V

R716 50

C727 .012uF/25V

+5V_ANALOG, CHN7,8

U708 8 4

C746 .10uF/50V

TALK_CH_7_8 7

R723 0

C738 10uF/35V

TO_CHN8_ALD 15

C737 2200pF/50V

R727 10.2K

R721 0

C735 2uF/35V

TO_CHN7_AUC 14

C736 2200pF/50V

R722 40.2K

C733 .10uF/50V

C734 10uF/25V

Vcc

FB700

+5V_CHN7,8

R717 2

+5V_ANALOG, CHN7,8

C728 47uF/16V

C729 10uF/35V

C730 .10uF/50V

C731 10uF/35V

C732 .10uF/50V

C739 47uF/16V

DGND

CAD GENERATED DRAWING

FILENAME: SEE SHT 1

DR	CK	APP	TITLE
BW			SCHEMATIC ANALOG I/O CARD CHANNEL 7,8 A/D AND D/A CONVERTER

DATE 011494

TELEX®
TELEX COMMUNICATIONS, INC.
MINNEAPOLIS, MINNESOTA

ADAM	90307510
MODEL	NEXT ASSY

SIZE D | DWG. NO. 90277510 | SHT 19 OF

BE .N

SHEET REV.	SHEET REVISION STATUS

REVISIONS							
LOC.	REV	DESCRIPTION	ECO NO	DRFT	C-KR	APP	DATE
	A	RELEASE	59954	BW	BW		11-94
	B	CHG PN C73-C77,L7,L9	60290	BW	BW		2-95
	C	REVISED PER ECO	60813	DP	DP		7-95

U1 U2 U3 U4 U5 U6

U6 U7

U7 U8 U9 U10 U11 U12 U13 U14

U15 U16 U17 U19 U20 U21 U22 U23 U24 U25 U26

U27 U28 U29 U30 U31 U32

CONNECTOR TO POWER PLANE

CAD GENERATED DRAWING
FILENAME: SEE SHT 1

DR	CK	APP
RW		

DATE 011494

TELEX®
TELEX COMMUNICATIONS, INC
MINNEAPOLIS, MINNESOTA

TITLE: ANALOG I/O CARD BYPASS CAPACITORS & INDUCTORS

ADAN	DWG NO
90307510	90307510
MODEL	NEXT ASSY

SIZE D SHT 20 OF